Serial No. 09/605,293
Docket MIO 0037 VA

At page 11, line 23 – page 12, line 3:

As shown in Fig. 2C, the source 56 and the drain 58 are formed by any conventional conductive doping technique currently in use in the art. Desirably, the source 56 and the drain 58 are formed by a self aligned technique. After the source 56 and the drain 58 have been formed, a layer 80 of a dielectric material 68 is formed on the gate oxide 54 and over the source 56 and drain 58. Typically, but not necessarily, the layer 80 will be a layer of an oxidized material and is provided at a thickness such that it serves as an insulating layer. Any material used in the art to form spacers would be useful for forming the layer 80 of dielectric material 68. Desirably, the dielectric material 68 is silicon dioxide or silicon nitride. The resulting field effect transistor 50 is shown in Fig. 2.

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At page 13, lines 2-9 should read:

amend

A thin film transistor 200 is shown in cross section in Fig. 5. The thin film transistor 200 includes an insulating substrate 202. A layer 204 of a semiconducting material 206 is formed on the surface of the substrate 202. A source region 208 and a drain region 210 are formed on the layer 204 of semiconducting material 206. A layer 212 of a dielectric material 214 is formed on the layer 204 of semiconducting material 206 and covers the source 208 and the drain 210. A layer 216 of a conducting material 218 is formed on the layer 212 of dielectric material 214 to form a gate electrode 220.

C3

IN THE CLAIMS

amend

10. (Twice Amended) A field effect transistor comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation, wherein said layer of silicon dioxide is free of metal contaminants;

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a layer of polycrystalline silicon formed on at least a portion of said layer of silicon dioxide, said layer of polycrystalline silicon having a smooth morphology; and

a source, a drain and a gate oxide formed in said semiconductor substrate with a gate electrode formed on said semiconductor substrate from said layer of polycrystalline silicon to form a field effect transistor.

11. (Twice Amended)A memory array comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, said layer of silicon dioxide having hydrogen ions implanted into at least a portion of said layer of silicon dioxide by plasma source ion implantation, wherein said layer of silicon dioxide is free of metal contaminants;

a layer of polycrystalline silicon formed over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted, said layer of polycrystalline silicon having a smooth morphology;

a plurality of memory cells arranged in rows and columns, each of said plurality of memory cells comprising at least one field effect transistor; [and]

a gate oxide, a source and a drain for each of said field effect transistors formed in said semiconductor substrate; and

a gate electrode for each of said field effect transistors formed on said semiconductor substrate from said layer of polycrystalline silicon.

12. (Twice Amended)A semiconductor wafer comprising:

a wafer including a semiconductor substrate, said wafer being divided into a plurality of die;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, on each of said plurality of die said layer of silicon dioxide having hydrogen ions implanted into at least a portion of said layer of